**Lab Number: 1**

**Section Number: 001**

**Names: Barak Barclay**

**Assigned Date: 02/04/2016**

**Due Date: 02/11/2016**

**Introduction:**

In this lab, 4 circuits will be written in Verilog emulating the INVERTER, AND, OR and the given circuit for part 4. These circuits will be written using code learned from class and simulated using the process learned in class for ModelSim.

**Part 1: Not Gate**

module Part1 (A,F);

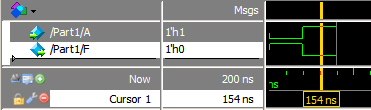
output F;

input A;

not G1 (F,A);

endmodule

|  |  |
| --- | --- |
| A | F |
| 0 | 1 |
| 1 | 0 |



**Part 2: And Gate**

module Part2 (A,B,F);

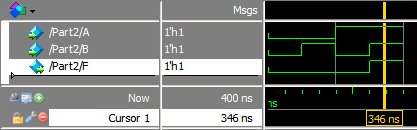
output F;

input A,B;

and G1 (F,A,B);

endmodule

|  |  |  |
| --- | --- | --- |
| A | B | F |
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |



**Part 3: Or Gate**

module Part3 (A,B,F);

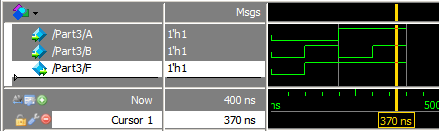
output F;

input A,B;

or G1 (F,A,B);

endmodule

|  |  |  |
| --- | --- | --- |
| A | B | F |
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |



**Part 4: Circuit Below**



module Part4 (A,B,C,F);

output F;

input A,B,C;

wire w1,w2;

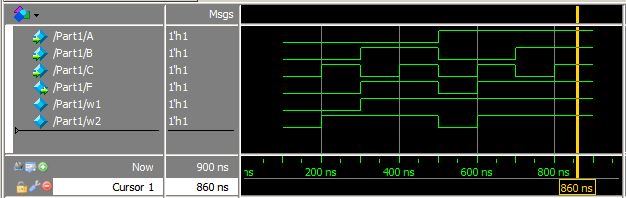
or G1 (w1,A,B);

or G2 (w2,B,C);

and G3 (F,w1,w2);

endmodule

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | C | W1 | W2 | F |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 1 |



**Conclusion:**

All gates and circuits were written in Verilog and simulated in ModelSIm using the code and process learned in class. If I need to elaborate more on the code, modules were created for each part, ports were initiated, wires were initiated, gates were defined with ports and wires, the module was ended, and the circuits were simulated using the process learned in class. If the process needs to be elaborated on, a project was created with a Verilog file, the modules for each part were written, the modules were saved, the modules were compiled, and the modules were simulated forcing the inputs to see every possible input combination.